In The Abstract:

Please cancel the original Abstract and replace it with the new Abstract attached hereto as Appendix A.

ABSTRACT OF THE DISCLOSURE

To speed up the operation of a decoder circuit, reduce the power consumption of the decoder circuit and increase the cycle, each circuit such as a buffer, a predecoder and a main decoder in the decoder circuit includes a semiconductor logic circuit in which the number of columns of transistors for pulling down at an output node is small, even if the number of inputs is large and the true and a complementary output signal having approximately the same delay time are acquired and the output pulse length of each circuit in the decoder circuit is reduced. With this arrangement, the operation of the decoder circuit can be sped up, the power consumption can be reduced, the cycles can be increased and, in a semiconductor memory, for example, access time and power consumption can be reduced and the cycles can be increased.